RESEARCH OPPORTUNITIES IN CRYSTALLINE SILICON PHOTOVOLTAICS FOR THE 21ST CENTURY

Harry A. Atwater
Thomas J. Watson Laboratory of Applied Physics
California Institute of Technology, Pasadena, CA 91125

Bhushan Sopori and Ted Ciszek
National Renewable Energy Laboratory
Golden, CO 80401-3393

Leonard C. Feldman
Department of Physics and Astronomy
Vanderbilt University
Nashville, TN 37235

James Gee
Sandia National Laboratories
Albuquerque, NM 87185-0752

Ajeet Rohatgi
School of Electrical Engineering
Georgia Institute of Technology
Atlanta, GA 30332

ABSTRACT

Crystalline silicon continues to be the dominant semiconductor material used for terrestrial photovoltaics. This paper discusses the scientific issues associated with silicon photovoltaics processing, and cell design that may yield cell and module performance improvements that are both evolutionary and revolutionary in nature. We first survey critical issues in "thick" crystalline silicon photovoltaics, including novel separations processes for impurity removal, impurity and defect fundamentals, interface passivation, the role of hydrogen. Second, we outline emerging opportunities for creation of a very different "thin-layer" silicon cell structure, including the scientific issues and engineering challenges associated with thin-layer silicon processing and cell design.

INTRODUCTION

Today's basic research advances in materials physics and materials synthesis and processing will provide the foundation for a large-scale industrial photovoltaics technology that appears likely to develop over the next 10-30 years. Over this time frame, the photovoltaics industry is expected to expand to a production level on the order of 10's GW/year worldwide, at which point it will be able to provide an important global source of clean energy. In this future, a prototypical photovoltaic manufacturing facility may be anticipated to produce on the order of 1 GW/year – and by simple considerations one can

project for example that such a plant will need to achieve a throughput on the order of 10 m^2 of modules per minute.

Crystalline silicon is very likely to maintain a quite significant role in photovoltaics technology over this time frame. Indeed, between 1992 and 1998, crystalline silicon has *expanded* its market share from 73% to 86% of the market relative to other photovoltaics technologies. Shipments of crystalline Si photovoltaics amounted to 132 MW per annum by 1998, and currently the Si photovoltaics industry is growing faster than its large cousin the microelectronics industry. Because of this large and continuing investment in silicon photovoltaics, it will be critical to address fundamental materials physics and materials synthesis issues related to crystalline silicon photovoltaics, since these basic research investments may enable further efficiency improvements and cost-reductions to occur.

Several significant scientific, technical and economic advantages accrue to crystalline Si:

- its device physics and materials physics issues are better understood than competing device materials. However very important basic materials physics issues remain outstanding for crystalline silicon photovoltaics. Moreover, critical issues related to minority carrier lifetime enhancement in multicrystalline or polycrystalline silicon are unlikely to be addressed by the microelectronics industry in the future.
- it is a serendipitous materials system: it has an extremely useful native oxide in SiO_2; as an elemental material it lacks stoichiometry problems; dopants such as Al and P can also play a role in gettering; silicon is mechanically robust relative to other semiconductors, facilitating cell processing.
- salubrity: it is a non-toxic, plentiful (and indeed even a nondepletable) material.
- There exists already a market-proven industrial manufacturing infrastructure.

Nevertheless, a crystalline silicon photovoltaics technology with GW/year-scale plants will likely look very different from today's technology. Cells and modules will need to be much easier to manufacture while maintaining high efficiency. Processes will have much higher throughputs, and will have significantly reduced material and energy inputs and reduced waste streams. High-throughput processing will be of critical importance. The silicon photovoltaics industry has historically adapted processes from the silicon microelectronics industry for manufacturing. The high throughputs required for the future GW/year-scale plants will require manufacturing paradigms more closely resembling other industries with similar processing throughputs – such as petrochemicals, plastics or glass products. Basic research opportunities exist for adapting high-throughput processes for crystalline-silicon. These include development of new cell and module designs that are more amenable to high-throughput processing, development of fundamentally-based process models to help guide research, and development of in-situ process monitors for better process control and optimization. More rapid processing of silicon will also require a more thorough understanding of silicon as a material, principally the effects of defects and impurities. Research in fundamentals of gettering, passivation, precipitate formation and dissolution will be necessary. As the demand and consumption of silicon material by the photovoltaics industry grow beyond that which

can be satisfied at the margins of silicon production for microelectronics, new methods of synthesis and purification of solar-grade silicon feedstock will be required. Also needed are more productive, less material consumptive methods for producing silicon substrates. In particular, thin substrates can reduce material consumption and improve manufacturing productivity. However thin substrates offer a number of challenges for fundamental research, including advanced surface and contact passivation, mechanical strength of thin substrates, and enhancement of optical absorption.

At the same time, significant research and manufacturing investments are also being made in thin film photovoltaic materials, such as amorphous silicon, CdTe, and copper indium diselenide and related chalcopyrite semiconductors. This is at least partly motivated by the potential manufacturing cost reductions that accompany processing of large, module-size sheets of absorber material rather than individual cells. For this reason, it is interesting to explore the possibility of a "thin layer" (1-30 μm thick) polycrystalline silicon cell or even perhaps a polycrystalline silicon/amorphous silicon tandem structure may compete favorably with the other thin film technologies.

Thus we can anticipate two kinds of basic research opportunities in crystalline silicon photovoltaics:

1. Rapid Evolutionary: research opportunities that will enable a rapid evolution from the cell designs and industrial processes of today to those that are usable in manufacturing plants with GW/year throughputs. Critical areas include impurity separation from Si feedstock, impurity and defect effects on cell performance, interface passivation issues at contacts, and the role of hydrogen. These are all currently issues facing Si photovoltaics, but they will have to be addressed anew in the future in the context of very high throughput manufacturing.

2. Revolutionary: research opportunities that will enable development of a new silicon photovoltaics technology based on thin-layer polycrystalline silicon growth in sheet form on low-cost substrates, most likely with very different cell designs and materials processing than that used in "thick" crystalline silicon photovoltaics today. This is currently a high-risk approach, since many uncertainties exist about cell structure and silicon processing approaches.

IMPURITY REMOVAL FROM SILICON FEEDSTOCK

The starting silicon for both photovoltaics and semiconductor integrated circuit applications is 99% pure metallurgical-grade (MG) Si. In wafer production for integrated circuit fabrication, chlorosilane purification and deposition steps increase the purity to more than adequate levels for photovoltaic use, but also increase the cost unacceptably. Hence the Si photovoltaics industry has been using reject material from integrated circuit polysilicon and single crystal production. But as production techniques improve and as the Si photovoltaics industry grows (~30% per annum) at a faster rate than the integrated

circuit industry, this material becomes rarer and more expensive. New sources of polysilicon will be needed [1,2]. Demand first exceeded supply in 1996. The present downturn in the integrated circuit industry has temporarily relieved the photovoltaics feedstock shortage, but projections by one of the largest polysilicon manufacturers indicate that demand for reject silicon will exceed the supply by a factor of 2 to 4 within 10 years. This does not represent a fundamental material shortage problem, since the technology and raw materials (quartzite, and coke) needed to make feed stock are in abundant supply. The issue is to supply feedstock with adequate –but not higher- purity in order to achieve acceptable feedstock cost.

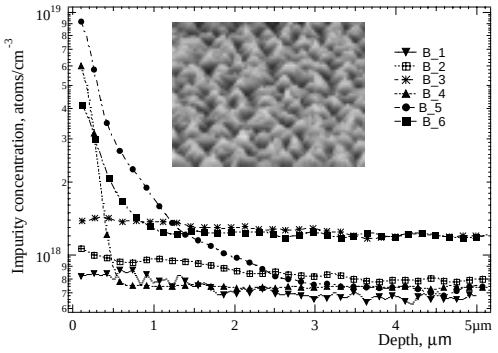


Figure 1. *Boron depth profiles at the surface of MG-Si subjected to various surface and annealing treatments. All treatments that included porous Si etching (inset) resulted in preferential accumulation of B at the surface (8).*

The trichlorosilane ($SiHCl_3$) distillation and reduction method used for over 95% of polysilicon production is very energy intensive, and it produces large amounts of waste, including a mix of environmentally damaging chlorinated compounds and about 80% of the initial MG-Si material. In addition, the feedstock produced by this method far exceeds the following preferred purity requirements of the photovoltaics industry: either B or P doping, with no compensation; resistivity at 25^{o}C greater than 1 ohm-cm; oxygen and carbon not exceeding saturation limits in the melt; and total non-dopant impurity concentration less than 1 ppma [3]. To meet the above-mentioned purity requirements, fresh approaches are needed to devise novel separation technologies that can extract B, Al, transition metal impurities and other impurities from impure silicon, but in a simple process. Some examples of new approaches that are in early stages of investigation include:

(i) use of electron beam and plasma treatments to remove impurities from MG-Si [4].

(ii) direct purification of granular MG-Si using repeated porous silicon etching, subsequent annealing, and surface impurity removal, as illustrated in Fig. 1 [5].

(iii) use of MG-Si and absolute alcohol as starting materials[6].

(iv) gaseous treatments of MG Si melts guided by thermochemical calculations [7].

(v) use of impurity partitioning when silicon is recrystallized from MG Si/metal eutectic systems [8].

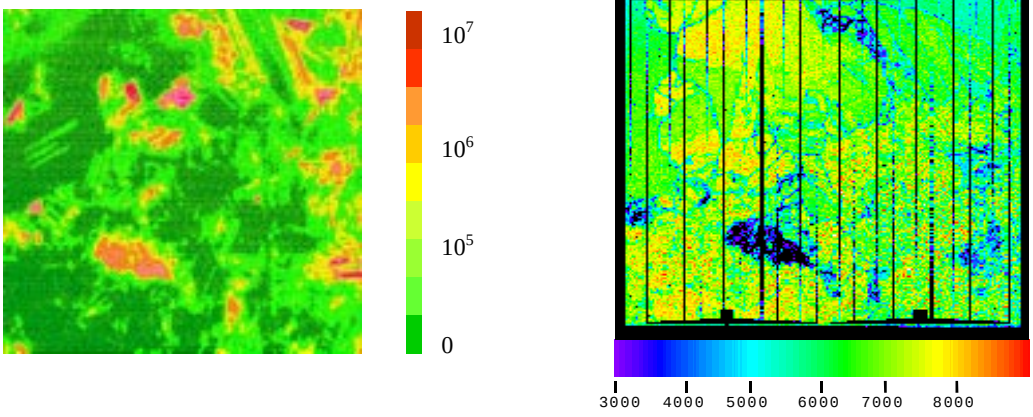
Approaches like these or other yet-to-be-determined innovative methods could have a major impact on the continued success and growth of the Si photovoltaics industry if a

feedstock purification method that is intrinsically simpler than current technology, and that yields adequate Si purity, can be developed.

IMPURITIES AND DEFECTS IN PHOTOVOLTAIC SI

The silicon photovoltaics industry uses low-cost substrates, which contain high concentrations of impurities and defects. In recent years, a variety of measures such as higher quality feedstock and better crucible quality have resulted in reduced metallic impurity content, to levels approaching 10^{14} cm^{-3}, while carbon and oxygen concentrations remain below saturation levels. Furthermore, there are ongoing attempts to improve the thermal conditions during the crystal growth processes that have yielded substrates with very low average defect density–typically $<10^5/cm^2$. However, it has been observed that as the defect density is reduced, the defects have a tendency to form clusters [9].

Figures 2(a) and 2(b) are defect and photocurrent maps showing the distribution of defects in a 25 cm^2 section of a commercial, multicrystalline silicon (mc-Si) wafer. The darker regions indicate higher defect densities. This figure indicates that a majority of the wafer has a low or zero dislocation density, while other regions have high concentrations of defects that are clustered together. Although the average value of the dislocation density in the entire wafer is about$10^5/cm^2$, defect clusters can be seen where the local defect density exceeds $10^7/cm^2$. Detailed analyses show that a defect cluster involves a series of long, intertwined dislocation loops. Because these loops and networks are high-energy defect configurations, they are thermally unstable and can change during device processing. Furthermore, the defect clusters can be efficient nucleation sites that can become decorated with impurity precipitates during crystal growth. This propensity for impurity decoration of a defect cluster has a strong bearing on how it affects the device performance.



(a) **(b)**

Figure 2. *In (a), a defect map of a 5-cm x 5-cm section of a commercial mc-Si wafer. The scale is in defects/cm^2. In (b), a photocurrent map of a solar cell fabricated on the wafer in (a), showing low response at defect clusters.*

Impurities and defects present in the as-grown substrate strongly affect its material quality. In general, the minority carrier diffusion length of as-grown substrates is low and varies spatially. The lowest minority carrier diffusion length occurs at defect clusters. Many approaches have been developed to mitigate the effects of defects and impurities. Impurity gettering is now extensively employed in silicon solar cell fabrication using phosphorous diffusion and Al alloying. Because these processes are generally combined with junction and contact formation processes, they need to be optimized for impurity gettering by maximizing the cell performance. It has been observed that impurity gettering does not occur uniformly over the entire wafer – the regions with zero or low defect density exhibit very effective gettering while defect cluster regions do not getter well [10]. This effect can be seen from Fig. 2(b), which is photoresponse map of a solar cell fabricated on the wafer shown in Fig. 2(a). The map was generated by a long wavelength excitation that produces a response proportional to the local minority carrier diffusion length. The low gettering efficiency in defect cluster regions has been attributed to the presence of precipitated metallic impurities. Some initial calculations have shown that it would require many hours of annealing at high temperatures exceeding 1000 °C to dissolve such precipitates. The presence of impurity-precipitates poses another problem: if cell processing is done at temperatures near or exceeding 900 °C, some of the precipitates dissociate to produce high concentrations of dissolved impurities that may not getter during the processing. In some cases this process can result in a degradation of the wafer quality [11].

Another approach to combat the influence of defects and impurities is to perform hydrogen passivation. It has been determined that hydrogen passivation is very effective in some materials such as edge-defined film growth silicon and string ribbon silicon and may not produce any significant effect on others. Recently, it has become possible to combine hydrogen passivation with PECVD nitride deposition used for antireflection coatings.

Theoretical analyses have shown that defect clusters limit the efficiency of many current commercial silicon solar cells. Defect cluster formation is not inherent to mc-Si growth but results from thermal stresses that occur high growth speeds. An interesting feature of defect clusters is that they primarily influence the voltage-related cell parameters without significantly lowering the photocurrent [9]. It is further shown that 18% efficiency cells can be fabricated if impurity precipitates within defect clusters can be gettered. This is currently a major effort within the DOE/NREL University Si Materials Research Program.

INTERFACE AND PASSIVATION ISSUES FOR SCREEN-PRINTED CONTACTS

One of the most difficult aspects of large-scale Si solar cell production is forming low-cost, high-quality front contacts. Screen-printing offers a simple, cost-effective method for contact formation that is consistent with the requirements for high throughput manufacturing [12,13]. The current problem with screen printing, however, is that the

throughput gains are attained at the expense of device performance. The technical literature shows considerable scatter in fill factor values (0.68 – 0.78) of screen-printed solar cells. In addition there are no clear guidelines for achieving high fill factors reproducibly, as the problem requires a compromise among a variety of complex design issues. Therefore, an approach for understanding the critical interface metallization issues relevant to optimizing screen-printed metallization is required, recognizing the fact that fill factor can be degraded by gridline resistance, contact resistance, and contact formation induced junction leakage and shunting.

A combination of modeling, fabrication, characterization is necessary to provide guidelines for achieving high fill factors (>0.78) on single crystal cells. The first step involves measuring metal resistivity as a function of firing temperature. For the Ag paste, metal resistivity decreases with the increase in firing temperature. In a recent study[13], for a firing time of 30 sec, the metal resistivity went below 3 μ-ohm-cm for firing temperatures above 700^{o}C. Model calculations indicated that 3 μ-ohm-cm is sufficient for grid design to achieve fill factor in excess of 0.78. The next step involves measuring shunt resistance (R_{sh}) as a function of firing temperature. In Ref. [13], it was found that for a 30 sec firing time, firing temperature should not exceed 730^{o}C to maintain R_{sh} in excess of 1 kΩ-cm^2, which is the second requirement for achieving fill factor in excess of 0.78. The third step involves tailoring the junction depth for 730^{o}C/30 min firing cycle in order to minimize junction leakage current (J_{02}). It was found that ~0.5 μm deep junction with a sheet resistance of ~40 ohms/sq was required for the above paste and firing condition to maintain J_{02} value below 10^{-8} A/cm^2 , which is the third requirement for achieving > 0.78 fill factor. The fourth step, a 400^{o}C/10 min forming gas anneal was found to be necessary for the above paste and firing conditions to reduce the series resistance to about 0.5 ohm-cm^2. Systematic optimization of the firing cycle and junction depth, coupled with a post contact forming gas anneal, resulted in 17% efficient cells with fill factors in the range of 0.78 – 0.796 on monocrystalline float zone silicon. This approach is sensitive to paste composition, junction depth, substrate quality and firing equipment or cycle.

The processes required for high quality contacts to low-cost materials may be quite different due to a high defect density, defect density non-uniformity, and paste/defect interactions. In a recent study[13] conducted on mc-Si from Eurosolare corporation using rapid beltline processing of emitter and screen printed contacts, a 40-45 ohms/sq emitter was formed at 925^{o}C in 6 min in a lamp heated beltline furnace. This resulted in a shallow junction depth of 0.25 μm, which makes devices vulnerable to screen-printed contact-induced junction shunting and leakage. In the course of investigating effects of paste composition on fill factor, it was found that impurities from the paste are able to penetrate the junction during a slow, prolonged firing cycle. It was found that rapid thermal processing during firing gave reasonable shunt and leakage current values but higher series resistance, preventing the fill factor from reaching 0.78. The best mc-Si cell efficiency achieved in this study was 15%, indicating the role of defects or paste/defect interaction in limiting the fill factor in mc-Si.

Since the fill factors achieved in these and other recent studies [14] are much greater than the fill factors (0.68 – 0.75) of current industrial cells [15], there is a need for

further development and technology transfer to bridge the gap between laboratory and industrial cells. Research should be conducted on fill factor loss mechanisms associated with paste chemistry and composition, defect inhomogeneity and defect/paste interactions in order to achieve large area screen-printed cells reproducibly with high fill factor (>0.78) on low-cost Si materials. These issues will become even more important for thinner silicon materials with more defects and smaller grain size. Development of a low-cost selective emitter, with <40 ohms/sq diffusion underneath the grid and > 80 ohms/sq between the gridlines, may lead to significant improvements in the performance of screen-printed cells. Finally, fine line printing, rapid thermal processing, and other novel low-cost contact formation techniques should be explored to reduce this dominant loss mechanism in the next generation of silicon cells.

THE BEHAVIOR OF HYDROGEN IN SILICON

The understanding of the behavior of hydrogen in all forms of silicon continues to evolve and is an essential component of the science underlying silicon-based photovoltaic technology. We describe here several interesting hydrogen-silicon phenomena that have emerged in the last few years that may provide research opportunities relevant to future silicon photovoltaics.

Hydrogen-silicon interactions have been found to be capable of cleaving macroscopic wafer-size thin (< 1 μm thick) layers of silicon from silicon crystals[16]. The hydrogen-induced cleaving process occurs through a series of steps in which hydrogen is implanted into silicon at high concentrations. A subsequent anneal initiates a planar cleaving process, resulting in a thin slab of silicon, either self-supporting or transferable to other substrates[16]. The process has been employed extensively for the implementation of silicon integrated circuit fabrication in a silicon-on-insulator configuration, and hydrogen-induced cleaving processes for preparation of large (200 mm) silicon-on-insulator substrates are now entering high-volume manufacturing. A series of experimental findings have revealed a detailed picture of the process. Bech-Nielsen et al.[17] have considered the dilute limit associated with isolated, hydrogen-coupled point defects in silicon. The results identify a series of defect complexes, which can be described as VH_n, a vacancy with n-attached hydrogen atoms passivating the dangling bonds. Chabal and co-workers [18,19] have used infrared spectroscopy to study the hydrogen-silicon system in the high concentration limit. The results illustrate the formation of hydrogen decorated platelets which eventually initiate a cleaving process, driven by the trapped, high-pressure gas. This process and the underlying science may play a significant role in further development of silicon-based photovoltaics employing thin crystalline silicon.

It has recently been discovered and is now well confirmed that deuterium passivation of the $Si\text{-}SiO_2$ interface renders a metal-oxide-semiconductor field-effect transistor (MOSFET) very resistant to trap generation by hot electron impingement [20,21]. This has lead to speculation on the effect of deuterium passivation in other silicon-based materials and devices. Indeed, the stability of deuterated a-Si based solar cells[22,23] and deuterated terminated porous silicon[24] has been found to improve with the use of the isotope and has shown enhanced stability against degradation due to light

and field exposure. The practical applicability of deuterium processing for all these systems is still under consideration. Nevertheless, it is clear that new understanding of the energetics and dynamics of hydrogen processes in silicon will emerge from this exciting research.

THIN LAYER SILICON PHOTOVOLTAICS

Although crystalline silicon technology, including both single crystal and multicrystalline, has been the dominant photovoltaics technology in the marketplace up to now, improvements in efficiency and reductions in cost/Watt for thin film technologies (based, e.g., on amorphous silicon, cadmium telluride and copper indium diselenide) strongly suggest that a significant part of the future of photovoltaics will be defined by thin films. This has motivated the exploration of an analogous approach for silicon, called here "thin-layer" silicon technology in which the silicon absorber layer is not self-supporting but is instead supported on a low-cost substrate (e.g., glass). A viable thin-layer silicon cell fabrication process, with its concomitant choice of low-cost substrate, must:

1. Yield module efficiencies of $\eta > 13$-14%.
2. Demonstrate potential for lower cost/area (< \$100/m^2) and/or cost/Watt (< \$2/Wp) than competing "thick" c-Si, a-Si and compound thin film technologies.
3. Have a fabrication throughput that can potentially equal or exceed process throughputs for "thick" c-Si and a-Si.
4. Enable use of low-cost (e.g., glass or ceramic) substrates.
5. Have potential to reach large-scale production on a reasonable time scale (10 years or less).

A thin-layer silicon module with 13-14 % efficiency will require: a sufficiently thick silicon layer (~5-30 μm) to achieve good red spectral response, a thin-layer cell with base diffusion length in excess of the base thickness, adequate grain size (~ 10-60 μm), control of intragranular defects such as point defect complexes, dislocations and stacking faults, and light trapping on one or both sides of the active layers.

Several groups have investigated low temperature thin-layer polycrystalline silicon formation on glass for photovoltaic applications [25-29]. Polycrystalline silicon cells of 9.2% efficiency formed by solid phase crystallization were demonstrated several years ago [26]. Recently, a group at Kaneka Corporation demonstrated a completely stable, JQA-confirmed polycrystalline silicon cell of 10.7% efficiency in a 2.0 μm thick silicon film grown by plasma-enhanced chemical vapor deposition (PECVD) on glass substrates [27]. These results establish the viability of thin crystalline silicon film materials for photovoltaics, and emphasize the extent to which careful attention to passivation and effective optical design in thin silicon cells can overcome the inherent disadvantage of crystalline silicon's indirect bandgap.

To realize a practical thin film silicon photovoltaics technology, several key problems and opportunities need to be addressed. For example, use of slightly thicker silicon films in the 5-20 μm range is expected to enable substantial improvements in cell

short circuit current, due to improved spectral response in the red and near infrared. However, growth of 5-20 μm silicon films is not currently practical due to low growth rates for the PECVD growth technique employed by Kaneka [3] and others. Kaneka reported a 7 μm minority carrier diffusion length extracted from cell spectral response data, implying impressive defect passivation in their 2 μm thick films with ~ 1 μm grain size. However, use of thicker silicon films in the 5-20 μm range will require substantially better quality material (with larger grain size and lower defect density) to enable minority carrier diffusion lengths greater than or equal to the film thickness. Moreover, since material quality typically degrades with increasing growth rate in low temperature vapor phase deposition processes, simultaneously achieving of high material quality and high growth rate for polycrystalline silicon presents a significant challenge.

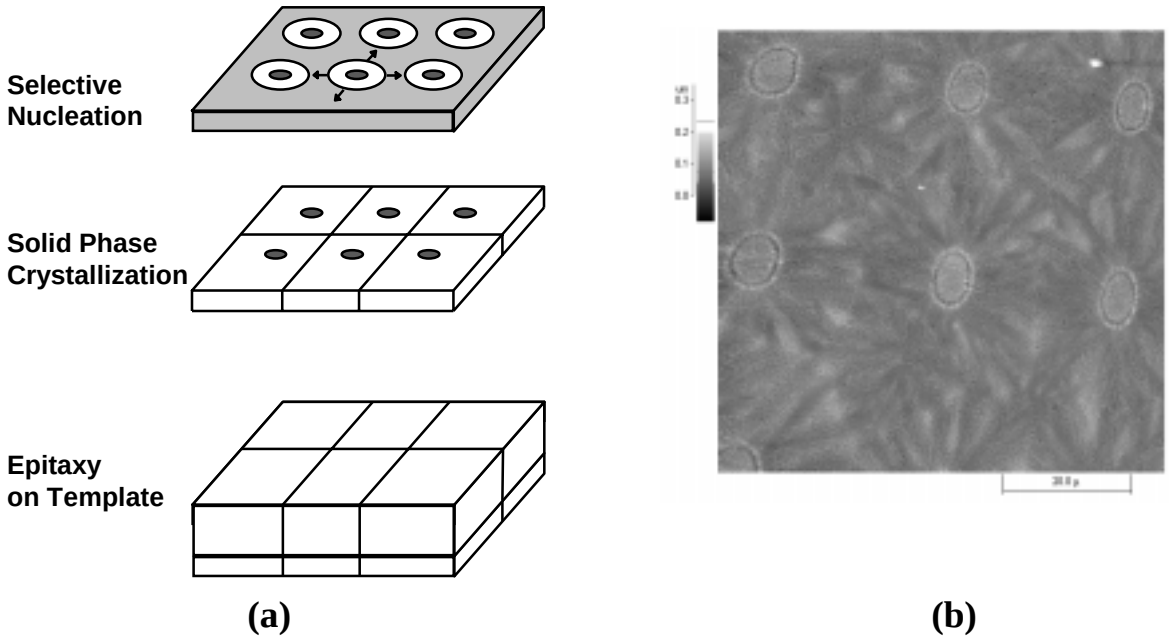


Figure 3. *In (a), schematic of low-temperature process for formation of large-grained thin-layer silicon on low-cost substrates via selection nucleation and solid phase epitaxy[28]. Selective nucleation of crystalline silicon in an amorphous silicon film forms a large-grained template for a thicker epitaxial silicon layer. In (b), atomic force micrograph of 0.5 μm crystal silicon grown at T = 490 ^{o}C on large-grained (~20 μm grain size) Ge template formed at T = 400^{o}C.*

Thus development of polycrystalline silicon cell processes and cell efficiencies that are competitive with other thin film technologies and "thick" crystalline silicon will require:

1. New approaches to improvement in thin-layer silicon material quality (increased grain size, lowered defect density) at the low temperatures demanded by use of low-cost substrates.

2. A breakthrough in thin-layer silicon growth rates, enabling polycrystalline silicon films of photovoltaically useful thickness to be grown while retaining high film quality.
3. A surface morphology with controlled roughness that enables enhanced optical absorption (i.e. "light-trapping), preferably formed during growth.

Broadly, approaches to thin-layer silicon growth can be divided into two classes: low temperature processes (T < 600 C) and high temperature processes (T > 900 C).

The biggest motivation for low temperature processes is the existence of low-cost substrates available in large quantity (e.g., soda-lime glass) and the technology base related to the prior existence of another large-area thin film silicon electronics technology, namely, flat-panel displays. The challenges facing low temperature thin-layer silicon processes are many, because key steps in conventional crystalline silicon technology, such as crystal growth and junction formation, are done at temperatures of T > 900 ^{o}C. The options for low-temperature crystal growth appear to be limited to solid phase crystallization, chemical vapor deposition or metal solution crystal growth. A large-grain silicon film made by a low temperature process, selective nucleation and solid phase epitaxy (SNSPE)[28] is depicted in Fig. 3.

For high temperature processes (T > 900 C), which may potentially enjoy greater flexibility in cell process design than low temperature processes, the biggest challenge is to identify a demonstrably low-cost, useful substrate. The options for substrate formation may include speciality glasses and glass-ceramic materials, or sintered pressed ceramic sheets of SiAlON or related materials. A large-grain silicon film made by a high temperature process, chemical vapor transport using the silicon tetraiodide reaction [29], is depicted in Fig. 4.

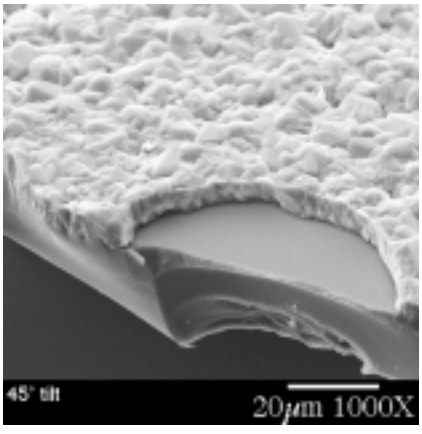


Figure 4. A 10 μm thick silicon film grown at T = 900 ^{o}C on high temperature glass substrates by chemical vapor transport, yielding a grain size of 5-10 μm and an effective minority carrier lifetime of 5 μsec.

]

CONCLUSIONS

Crystalline silicon will remain an *important and possibly dominant* technology in photovoltaics over the next 10-30 years, owing to its well-recognized desirable material properties and also to its established infrastructure for photovoltaic manufacturing.

Basic research needs for the 21st century include development of new separations processes for removing impurities from silicon feedstock, improved understanding of defect and impurity interactions in multicrystalline silicon, the development of novel, orientation-independent processes for light trapping, surface passivation at contacts and other interfaces in thin Si structures, and improved understanding of the role of hydrogen in crystalline silicon.

Thin-layer silicon fabrication is now in the earliest stages of research, and the most important challenge at present is to grow a thin-layer silicon absorber that can achieve adequate photovoltaic performance on a low-cost substrate in a cost-effective manner. This will require new understanding of the kinetic limits to vapor phase Si deposition rates at low to intermediate temperatures. It will also require new understanding of the relation between vapor phase epitaxial crystal growth and defect generation. Other important issues for thin-layer silicon parallel those that are critical for thicker crystalline silicon. Building upon experience gained from today's crystalline silicon photovoltaics technology, achievement of good quality thin-layer silicon material on low-cost substrates will guide the way to progress in development of complete thin-layer silicon cell and module processes.

REFERENCES

1. M.G. Mauk, P.E. Sims, and R.B. Hall, "Feedstock for Crystalline Silicon Solar Cells," American Institute of Physics Conf. Proc., 404, 21 (1997).
2. K.M. Mitchell, "The Status of Polysilicon Feedstock," American Institute of Physics Conf. Proc., 462, 362 (1998).
3. Summary of the Panel Discussions of the Sixth Workshop on the Role of Impurities and Defects in Silicon Device Processing, NREL/SP-413-21640, September 1996.
4. N. Nakamura, M. Abe, K. Hanazawa, H. Baba, N. Yuge, and Y. Kato, "Development of NEDO Melt-Purification Process for Solar Grade Silicon and Wafers," Proc. 2nd World Conf. on Photovoltaic Solar Energy Conversion, 1193 (1998).
5. P. Menna, Y.S. Tsuo, M.M. Al-Jassim, S.E. Asher, R. Matson, and T.F. Ciszek, "Purification of Metallurgical-Grade Silicon by Porous-Silicon Etching," Proc. 2nd World Conf. on Photovoltaic Solar Energy Conversion, 1232 (1998).
6. Y.S. Tsuo, J.M. Gee, P. Menna, D.S. Strebkov, A. Pinov, and V. Zadde, "Environmentally Benign Silicon Solar Cell Manufacturing," Proc. 2nd World Conf. on Photovoltaic Solar Energy Conversion, 1199 (1998).
7. J. M. Gee, P. Ho, J. Van Den Avyle, and J. Stepanek, "Some Thermochemical Calculations on the Purification of Silicon Melts," 8th Workshop on Crystalline Silicon Solar Cell Materials and Processes, August, 1998.
8. T.H. Wang and T.F. Ciszek, "Impurity segregation in LPE growth of silicon from Cu-Al solutions," Journal of Crystal Growth 174 (1997) 176-181.
9. B. L. Sopori, Proc. ICDS-19, Trans Tech Pub., Edited by G. Davies and M.H. Nazare, 527 (1997).
10. B. L. Sopori, L. Jastrzebski, T. Y. Tan, and S. Narayanan, Proc. 12th PVSEC, 1003(1994).

11. B. L. Sopori, W. Chen, T.Y. Tan, and P. Plekhanov, National Center for Photovoltaics, Photovoltaics Program Review, AIP Conference Procd. 462, 341 (1998).
12. J. Nijs et. al., "Latest Efficiency Results with the Screenprinting Technology and Comparison with Buried Contact Structure," Proceedings of the 1st World Conference on Photovoltaic Energy Conversion, Hawaii, 1242, (1994).
13. A. Rohatgi et. al., "Understanding and Implementation of Rapid Thermal Technologies for Low-Cost High Efficiency Silicon Solar Cells," to be published in IEEE Transaction on Electron Devices, (1999).
14. F. Duernickx et. al, "Simplified and Efficient Screen Printing Process for Multicrystalline Silicon Solar Cells Based on Firing Through Silicon Nitride," Proceedings of 14th European Photovoltaic Solar Energy Conference, Barcelona, Spain, 792, (1997).
15. T. Koval, J. Wohlgemuth, and B. Kinsey, "Dependence of Cell Performance on Wafer Thickness for BSF and non-BSF Cells, "Proceedings of 25th IEEE Photovoltaic Specialists Conference, Washington, D.C., 505, (1996).
16. M. Bruel, Nucl. Instr. and Meth. **B108**, 313 (1996)
17. B.Bech Nielsen, L. Hoffmann and M. Budde, Matls Sci. and Eng. **B36**, 259 (1996).
18. M.K. Weldon, V. Marsico, Y.J.Chabal, S.B. Christman, E.E. Chaban, D.C. Jacobson, J.B. Sapjeta, A. Pinczuk, B.S. Dennis, A.P. Mills, C.A. Goodwin, and C.-M. Hsieh, Proc 1996 IEEE Int. SOI Conf., 150 (1996).
19. M.K. Weldon, Y.J. Chabal, D.R. Hamann, S. B. Christman, E.E. Chaban and L.C. Feldman, J. Vac. Sci. and Tech. **B14**, 3095, (1996).
20. J. W. Lyding, K.Hess, and I.C. Kizilyalli, Appl. Phys Let. **68**, 2526 (1996).
21. K. Hess, I.C. Kizilyalli and J.W. Lyding, IEEE Trans. Elec. Dev., **45,** 406 (1998).
22. J.H. Wei, M.S. Sun and S.C. Leee, Appl. Phys. Let., **71,** 1498 (1997).
23. S. Sugiyama, J. Yang, and S. Guha, Appl. Phys. Let. **70**, 378, (1997).
24. T. Matsumoto, Y. masumoto, T, Nakagawa, M. Hashimoto, K. Ueno, and N. Koshida, Jpn. J. Appl. Phys., **36**, L1089 (1997).
25. See for example: K. Yamamoto, A. Nakajima, T. Suzuki, M. Yoshimi, H. Nishio and M. Izumina, Jpn.J. Appl. Phys. 33 L1751 (1994); R. Brendel, R. Bergmann, P. Lolgen, M. Wolf, and J. Werner, Appl. Phys. Lett. 70 390 (1997); C.M Chen, C.M. Yang and H.A. Atwater, presented at 7th NREL Workshop on Defects and Impurities in Silicon Device Processing, Vail CO, 1997; Z. Shi and S. Wenham, Prog. Photovoltaics, 2 153 (1994).
26. T. Matsuyama, N. Terada, T. Baba, T. Sawada, S. Tsuge, K. Wakisaka, and S. Tsuda, J. Non-cryst. Solids **200**, 940 (1996).
27. K. Yamamoto, M. Yoshimi, T. Suzuki, Y. Tawada, T. Okamoto and A. Nakajima, presented at Spring 1998 Materials Research Society Meeting, San Francisco, CA; published in Proceedings of the EPVSEC, Barcelona, p. 1018 (1997).

28. "*Polycrystalline Si Films Fabricated by Low Temperature Selective Nucleation and Solid Phase Epitaxy Process*," C. M. Chen, and H. A. Atwater, in Thin-Film Structures for Photovoltaics, edited by E. D. Jones, J. Kalejs, R. Noufi, and B. L. Sopori, Mater. Res. Soc. Proc. 485, 67-72 (1998) .
29. T.F. Ciszek, private communication.